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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/764,595	01/18/2001	Christopher A. Krygowski	POU920000158US1	6652

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/764,595	Applicant(s) KRYGOWSKI ET AL.	
	Examiner Chat C. Do	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because the abstract exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

Re claim 6, the word "an" in line 2 should be "a".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the limitation "the minimum number" in line 5 lacks an antecedence basis. For examination purposes, the examiner considers this limitation as "a minimum number". Thus, claims 2-11 are also rejected for being dependent on the rejected base claim 1.

Re claim 12, the limitation "the internal floating point format" in line 8 lacks an antecedence basis. For examination purposes, the examiner considers this limitation as "an internal floating point format". Thus, claims 13-17 are also rejected for being dependent on the rejected base claim 12.

Re claim 18, the limitation "the instant floating point architecture" in line 8 lacks an antecedence basis. For examination purposes, the examiner considers this limitation as "an instant floating pint architecture".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4 and 6-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Schwarz et al. (U.S. 5,687,106).

Re claim 1, Schwarz et al. disclose in Figure 1 computer system for supporting a plurality of floating point architectures (col. 3 lines 20-27), each floating point architecture having at least one format (IEEE 754 and IBM S/390), the system

comprising: a floating point unit (Figure 5) having an internal data-flow (18) according to an internal floating point format for performing floating point operations in the internal format (col. 3 lines 27-31), wherein the internal format has a number of exponent bits which is at least the minimum number required to support each of the plurality of floating point architectures and the internal format has a number of fraction bits which is at least the minimum number required to support each of the plurality of floating point architectures (col. 1 lines 57-64); and a converter (25 and 26) for converting an exponent value corresponding to each one of the plurality of floating point architectures into the internal floating point format such that an operand of any one of the plurality of floating point architectures input to the floating point unit is converted into the internal floating point format for operation by the floating point unit, and the result of the operation is converted back (24) into the one of the plurality of floating point architectures by converting an exponent value corresponding to the internal floating point format into the one of the plurality of floating point architectures (col. 1 lines 63-65).

Re claim 2, Schwarz et al. further disclose in Figure 1 the fraction bits corresponding to each of the plurality of floating point architectures are used by the floating-point unit in an unconverted state (table 1).

Re claim 3, Schwarz et al. further disclose in Figure 1 the plurality of floating point architectures include IBM®-S/390© hexadecimal floating point architecture and IEEE-754 binary floating point architecture (col. 1 lines 57-62).

Re claim 4, Schwarz et al. further disclose in Figure 1 the converter determines a sign bit; and normalizes (22) a resulting binary floating-point number (output of 18) according to at least one of IBM®-S/390® and IEEE-754 normalization modes (24).

Re claim 6, Schwarz et al. further disclose in Figure 1 the plurality of floating point architectures includes a binary architected format and a hexadecimal architected format (col. 1 lines 57-64), and the internal format is a binary internal format (col. 1 lines 66-67 and col. 2 lines 1-2).

Re claim 7, Schwarz et al. further disclose in Figure 1 the binary internal format has a common predetermined fraction type corresponding to both of the hexadecimal and the binary architected formats (col. 3 lines 34-37).

Re claim 8, Schwarz et al. further disclose in Figure 1 the numbers represented in the binary internal format corresponding to each of the hexadecimal architected format and the binary architected format (col. 1 lines 57-64), respectively, each have predetermined bias types that differ in the locations of the implied radix points (table 1).

Re claim 9, Schwarz et al. further disclose in Figure 1 the binary internal format has a nonzero positive integer number M of exponent bits and a bias equal to $2^{(M-1)} - 1$, where M is the length of the internal exponent field (col. 2 lines 58-59).

Re claim 10, Schwarz et al. further disclose in Figure 1 the plurality of floating point architectures includes a binary architected format and a hexadecimal architected format, the internal format is a binary internal format, and the converter comprises: a first converter portion (25 and 26) that converts the hexadecimal architected format to the binary internal format, and converts the binary architected format to the binary internal

format; and a second converter portion (24) that converts the binary internal format into the binary architected format, and converts the binary internal format into the hexadecimal architected format.

Re claim 11, Schwarz et al. further disclose in Figure 1 the first converter portion comprises an input format conversion multiplexor and input format conversion control, and the second converter portion comprises an output format conversion multiplexor and output format conversion control (27 and 28).

Re claim 12, it is a unit claim of claim 10. Thus, claim 12 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 13, Schwarz et al. further disclose in Figure 1 an operand of the first floating point architecture type is directly converted into the internal floating point format by the first converter for operation by the floating point unit with no additional delay, and therein an operand of the second floating point architecture type is converted into the internal floating point format by the second converter with no additional delay (there is no delay in between 10 to 25 and 26).

Re claim 14, Schwarz et al. further disclose in Figure 1 data in the internal floating point format is directly converted into data of the first floating point architecture by the third converter (15) with no additional delay, and wherein data in the internal floating point format is directly converted into data of the second floating point architecture by the fourth converter (16) with no additional delay.

Re claim 15, Schwarz et al. further disclose in Figure 1 the internal floating-point format has a minimum nonzero positive number of exponent bits, N, to support both first and second floating-point architectures (col. 3 lines 32-40).

Re claim 16, Schwarz et al. further disclose in Figure 1 the internal floating-point format has a single fraction type corresponding to the fraction portions of both the first and second floating point architectures (col. 3 lines 32-40).

Re claim 17, Schwarz et al. further disclose in Figure 1 the internal format has the same fraction type as both of the first and second floating point architectures (col. 3 lines 32-40).

Re claim 18, it is a method claim of claim 10. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 10.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Schwarz et al. (U.S. 5,687,106).

Re claim 5, Schwarz et al. do not disclose the internal floating-point format is a binary format that has a 16-bit exponent biased by 32,768, a sign bit, and a 56-bit fraction. However, Schwarz et al. disclose in table 1 a chart that supports all formats.

From the chart, the 16-bit average minimum exponent size is required to support all the exponents size, the bias is $2^{15} = 32,768$, one bit is the sign bit, and a 56-bit fraction is required to support the hex short, hex long, binary single, and binary double. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a internal floating-point format is a binary format that has a 16-bit exponent biased by 32,768, a sign bit, and a 56-bit fraction as seen in Schwarz et al.'s table 1 because it would enable to simplify the system hardware and improve the performance to support the hexadecimal short, hexadecimal long, binary single, and binary double formats.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,055,554 to Schwarz discloses a floating-point binary quad word format multiply instruction unit.

b. U.S. Patent No. 5,825,678 to Smith discloses a method and apparatus for determining floating-point data class.

c. U.S. Patent No. 5,687,359 to Smith Sr. discloses a floating-point processor supporting hexadecimal and binary modes using common instructions with memory storing a pair of representations for each value.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

July 23, 2003

CHUONG DINH NGO
PRIMARY EXAMINER